BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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| In re Application of: Basso et al. | : | Before the Examiner: Zhu, Bo Hui Alvin |
| Serial No.: 10/706,235 | : | Group Art Unit: 2619 |
| Filing Date: November 12, 2003 | : | |
| Title: REDUCING MEMORY ACCESSES IN PROCESSING TCP/IP PACKETS | : | IBM Corporation<br>IP Law Dept. YXSA/Bldg. 002<br>3039 Cornwallis Road<br>P.O. Box 12195<br>Research Triangle Park, NC 27709 |

# APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
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## I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, which is the assignee of the entire right, title and interest in the above-identified patent application.

## II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

## III. STATUS OF CLAIMS

Claims 1-15 are pending in the Application. Claims 1-15 stand rejected. Claims 1-15 are appealed.

## IV. STATUS OF AMENDMENTS

Appellants have not submitted any amendments following receipt of the final office action with a mailing date of October 17, 2007.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 1:

In one embodiment of the present invention, a method for processing packets of data comprises the step of receiving a packet of data. Specification, page 13, lines 13-15; Figure 4, step 401. The method further comprises storing a payload of the packet of data in a buffer. Specification, page 13, lines 17-20; Figure 4, step 402. Further, the method comprises reading a header of the packet of data to extract a value. Specification, page 13, lines 21-24; Figure 4, step 403. Furthermore, the method comprises indexing in a table storing a list of transport control blocks using the value. Specification, page 13, lines 24-28; Figure 4, step 404. Additionally, the method comprises performing a lock operation on a transport control block in an indexed entry in the table. Specification, page 14, lines 1-4; Figure 4, step 405. Further, the method comprises performing a read operation on the transport control block. Specification, page 14, lines 5-9; Figure 4, step 406. In addition, the method comprises transmitting a notification to an application to read the payload, where the notification comprises an address of the transport control block. Specification, page 14, lines 10-12; Figure 4, step 407. Furthermore, the method comprises transmitting the payload of the received packet of data to the application whereby the application does not perform a lock, read, write or unlock operation on the transport control block. Specification, page 14, lines 16-27; Figure 4, step 409.

Independent Claim 6:

In one embodiment of the present invention, a computer program product embodied in a machine readable medium for processing packets of data comprises the programming step of receiving a packet of data. Specification, page 12, lines 4-15;

Specification, page 13, lines 13-15; Figure 4, step 401. The computer program product further comprises the programming step of storing a payload of the packet of data in a buffer. Specification, page 12, lines 4-15; Specification, page 13, lines 17-20; Figure 4, step 402. Further, the computer program product comprises the programming step of reading a header of the packet of data to extract a value. Specification, page 12, lines 4-15; Specification, page 13, lines 21-24; Figure 4, step 403. Furthermore, the computer program product comprises the programming step of indexing in a table storing a list of transport control blocks using the value. Specification, page 12, lines 4-15; Specification, page 13, lines 24-28; Figure 4, step 404. Additionally, the computer program product comprises the programming step of performing a lock operation on a transport control block in an indexed entry in the table. Specification, page 12, lines 4-15; Specification, page 14, lines 1-4; Figure 4, step 405. Further, the computer program product comprises the programming step of performing a read operation on the transport control block. Specification, page 12, lines 4-15; Specification, page 14, lines 5-9; Figure 4, step 406. In addition, the computer program product comprises the programming step of transmitting a notification to an application to read the payload, where the notification comprises an address of the transport control block. Specification, page 12, lines 4-15; Specification, page 14, lines 10-12; Figure 4, step 407. Furthermore, the computer program product comprises the programming step of transmitting the payload of the received packet of data to the application whereby the application does not perform a lock, read, write or unlock operation on the transport control block. Specification, page 12, lines 4-15; Specification, page 14, lines 16-27; Figure 4, step 409.

Independent Claim 11:

In one embodiment of the present invention, a system comprises a communications adapter configured to communicate with an outside network, where the communications adapter receives a packet of data from the outside network. Specification, page 10, lines 14-18; Specification, page 13, lines 13-15; Figure 2, element 201; Figure 4, step 401. The system further comprises a memory unit

coupled to the communications adapter, where the memory unit stores a table listing a plurality of transport control blocks. Specification, page 11, lines 7-15; Figure 2, element 206. Further, the system comprises a TCP protocol stack running on the communications adapter. Specification, page 10, lines 18-24; Figure 2, element 203. Additionally, the system comprises a TCP application running on the communications adapter. Specification, page 10, line 25 – page 11, line 4; Figure 2, element 204. The TCP protocol stack is configured to perform the programming step of storing a payload of the packet of data in a buffer in the memory unit. Specification, page 13, lines 17-20; Figure 4, step 402. Additionally, the TCP protocol stack is configured to perform the programming step of reading a header of the packet of data to extract a value. Specification, page 13, lines 21-24; Figure 4, step 403. Additionally, the TCP protocol stack is configured to perform the programming step of indexing in the table using the value. Specification, page 13, lines 24-28; Figure 4, step 404. Furthermore, the TCP protocol stack is configured to perform the programming step of performing a lock operation on a transport control block in an indexed entry in the table. Specification, page 14, lines 1-4; Figure 4, step 405. Further, the TCP protocol stack is configured to perform the programming step of performing a read operation on the transport control block. Specification, page 14, lines 5-9; Figure 4, step 406. Additionally, the TCP protocol stack is configured to perform the programming step of transmitting a notification to the TCP application to read the payload, where the notification comprises an address of the transport control block. Specification, page 14, lines 10-12; Figure 4, step 407. Further, the TCP protocol stack is configured to perform the programming step of transmitting the payload of the received packet of data to the TCP application whereby the TCP application does not perform a lock, read, write or unlock operation on the transport control block. Specification, page 14, lines 16-27; Figure 4, step 409.

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Appellants' Background (pages 1, line 14 – page 4, line 22 of

Appellants' Specification) in view of Bezzant et al. (U.S. Patent No. 6,014,717) (hereinafter "Bezzant").

VII. ARGUMENT

A. Claims 1-15 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Appellants' Background in view of Bezzant.

1. Appellants' Background and Bezzant, taken singly or in combination, do not teach at least the following claim limitations.

a. Claims 1, 6 and 11 are patentable over Appellants' Background in view of Bezzant.

Appellants respectfully assert that Appellants' Background and Bezzant, taken singly or in combination, do not teach "transmitting said payload of said received packet of data to said application whereby said application does not perform a lock, read, write or unlock operation on said transport control block" as recited in claim 1 and similarly in claims 6 and 11. The Examiner asserts that Bezzant teaches the above-cited claim limitation. Office Action (10/17/2007), page 3. Appellants respectfully traverse.

Bezzant instead teaches a PCMCIA host adapter includes the capability to master a non-DMA system bus and control a DMA data transfer between a DMA capable peripheral and the internal system memory. Abstract. Bezzant further teaches that a peripheral can be coupled to the system through a PCMCIA card plugged into a PCMCIA expansion slot. Abstract. Bezzant additionally teaches that a DMA controller coupled to the PCMCIA expansion slots through a PCMCIA bus controls a DMA transfer between the internal system memory and the peripheral. Abstract. Furthermore, Bezzant teaches that a bus master disables the CPU and takes control of the system bus during a DMA data transfer. Abstract.

There is no language in Bezzant that teaches transmitting the payload of a received packet of data. Neither is there any language in Bezzant that teaches transmitting the payload of a received packet of data to an application. Neither is

there any language in Bezzant that teaches transmitting the payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation. Neither is there any language in Bezzant that teaches transmitting the payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1, 6 and 11, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

In response to Appellants' above arguments, the Examiner cites column 1, lines 16-38 of Bezzant as teaching the above-cited claim limitation. Office Action (10/17/2007), page 4. Appellants respectfully traverse.

Bezzant instead teaches that during a computer's operation it is often necessary for data to be transferred between an external mass storage device, such as a magnetic disk or a magnetic tape, and the internal memory within the computer system. Column 1, lines 18-21. Bezzant further teaches that when using a direct memory access (DMA) technique, it is possible to bypass the microprocessor during such transfers and allow data to be transferred directly between the peripheral device and internal system memory, thus improving speed and reducing latency of the transfer, and correspondingly improving efficiency of the system. Column 1, lines 25-30. Bezzant additionally teaches that during a DMA transfer, the microprocessor gives up control of the system bus and a DMA controller takes control of the system bus to manage the transfer directly between the peripheral device and the internal system memory. Column 1, lines 36-39.

Hence, Bezzant teaches using the direct memory access (DMA) technique where data is transferred directly between a peripheral device and the internal system memory. Bezzant further teaches that during a DMA transfer, the microprocessor gives up control of the system bus and a DMA controller takes control of the system

bus to manage the transfer directly between the peripheral device and the internal system memory.

There is no language in the cited passage that teaches transmitting the payload of a received packet of data. Neither is there any language in Bezzant that teaches transmitting the payload of a received packet of data to an application. Neither is there any language in Bezzant that teaches transmitting the payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation. Neither is there any language in Bezzant that teaches transmitting the payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1, 6 and 11, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Instead, the Examiner focuses on DMA techniques which is not related to the above-cited claim limitations. Using a DMA controller instead of a microprocessor to manage the transfer directly between the peripheral device and the internal system memory does not imply the teaching of transmitting a payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block. How does the teaching of the DMA technique imply the teaching of transmitting a payload of a received packet of data to an application? How does the teaching of the DMA technique imply the teaching of transmitting a payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block?

The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that the teaching of the DMA technique necessarily implies the teaching of transmitting a payload of a received packet of data to an application

whereby the application does not perform a lock, read, write or unlock operation on the transport control block. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that the teaching of the DMA technique necessarily implies the teaching of transmitting a payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided any such objective evidence, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1, 6 and 11. M.P.E.P. §§2112.

Furthermore, the Examiner is ignoring claim language in claims 1, 6 and 11. The Examiner does not discuss the following limitations: transmitting a payload of a received packet of data; transmitting a payload of a received packet of data to an application; transmitting the payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation; transmitting the payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block. For instance, what is the Examiner referring to as the claimed application? Is the Examiner referring to the microprocessor? If so, how can a microprocessor be the claimed application? Further, if the Examiner is referring to the internal system memory as allegedly teaching the claimed transport control block, the Examiner needs to provide evidence that Bezzant teaches that the internal system memory of Bezzant stores transport control blocks. The Examiner cannot ignore claim language. All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); M.P.E.P. §2143.03. Since the Examiner has not cited to any passage in Bezzant as teaching the above-cited claim limitations, the Examiner has not established a *prima facie* case of obviousness in rejecting claims 1, 6 and 11. M.P.E.P. §2143.

b. Claims 2-5, 7-10 and 12-15 are patentable over Appellants' Background in view of Bezzant for at least the above-stated reasons that claims 1, 6 and 11, respectively, are patentable over Appellants' Background in view of Bezzant.

Claims 2-5 each recite combinations of features of independent claim 1, and hence claims 2-5 are patentable over Appellants' Background in view of Bezzant for at least the above-stated reasons that claim 1 is patentable over Appellants' Background in view of Bezzant.

Furthermore, claims 7-10 each recite combinations of features of independent claim 6, and hence claims 7-10 are patentable over Appellants' Background in view of Bezzant for at least the above-stated reasons that claim 6 is patentable over Appellants' Background in view of Bezzant.

Additionally, claims 12-15 each recite combinations of features of independent claim 11, and hence claims 12-15 are patentable over Appellants' Background in view of Bezzant for at least the above-stated reasons that claim 11 is patentable over Appellants' Background in view of Bezzant.

2. Examiner's reasoning for modifying Appellants' Background with Bezzant to incorporate the missing claim limitations of claims 1, 6 and 11 is insufficient to establish a *prima facie* case of obviousness.

Most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Obviousness is determined from the vantage point of a hypothetical person having ordinary skill in the art to which the patent pertains. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Therefore, an Examiner may often find every element of a claimed invention in the prior art. *Id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See Id.* In order to establish a *prima facie* case of obviousness, the Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of

the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner must provide articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (cited approvingly in *KSR International Co. v. Teleflex Inc.*, 82 U.S.P.Q.2d 1385, 1396 (U.S. 2007)).

As understood by Appellants, the Examiner admits that Appellants' Background does not teach "transmitting said payload of said received packet of data to said application whereby said application does not perform a lock, read, write or unlock operation on said transport control block" as recited in claim 1 and similarly in claims 6 and 11. Office Action (10/17/2007), page 2. The Examiner asserts that Bezzant teaches the above-cited claim limitation. *Id.* at page 3. The Examiner's reasoning for modifying Appellants' Background with Bezzant to include the above-cited claim limitation is "so as to improve speed and reduce latency in transferring data." *Id.* The Examiner's reasoning is insufficient to establish a *prima facie* case of obviousness in rejecting claims 1-15.

The Examiner appears to be relying upon column 1, lines 16-38 of Bezzant as support for the Examiner's reasoning for modifying Appellants' Background with Bezzant to include the above-cited claim limitation. Office Action (10/17/2007), page 5. As stated above, column 1, lines 16-38 of Bezzant teaches using the direct memory access (DMA) technique where data is transferred directly between a peripheral device and the internal system memory. Further, column 1, lines 16-38 of Bezzant teaches that during a DMA transfer, the microprocessor gives up control of the system bus and a DMA controller takes control of the system bus to manage the transfer directly between the peripheral device and the internal system memory. There is no language in Bezzant (and in particular column 1, lines 16-38 of Bezzant) that makes any suggestion to transmit a payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block (missing claim limitation) in order to improve speed and

reduce latency in transferring data (Examiner's reasoning). Bypassing the microprocessor by using a DMA controller to transfer data between the peripheral device and the internal system memory does not enable one to transmit a payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block as suggested by the Examiner. How does transferring data between the peripheral device and the internal system memory relate to transmitting a payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block? The Examiner's source of reasoning (column 1, lines 16-38) does not provide reasons as to why one skilled in the art would modify Appellants' Background to include the above-cited missing claim limitation of claims 1, 6 and 11. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1, 6 and 11. *KSR International Co. v. Teleflex Inc.*, 82 U.S.P.Q.2d 1385, 1396 (U.S. 2007).

Further, the Examiner' reasoning ("so as to improve speed and reduce latency in transferring data") does not provide reasons, as discussed further below, that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify Appellants' Background to include the above-indicated missing claim limitation of claims 1, 6 and 11. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-15. *KSR International Co. v. Teleflex Inc.*, 82 U.S.P.Q.2d 1385, 1396 (U.S. 2007); *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

Why would the reason to modify Appellants' Background to transmit the payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block (missing claim limitation) be so as to improve speed and reduce latency in transferring data? What is the rationale connection between the Examiner's reasoning (reducing latency in transferring data) and transmitting the payload of a received packet of data to an application whereby the application does not perform a lock,

read, write or unlock operation on the transport control block (missing claim limitation)? The Examiner states:

> Since a lock, read, write or unlock operations on transport control block as claimed are essentially operations performed by the microprocessor when accessing the memory. By bypassing the microprocessor as suggested in the Bezzant reference, it would therefore improve the speed and latency in accessing data from memory. Office Action (10/17/2007), page 5.

The Examiner has not provided any basis in fact and/or technical reasoning to support the assertion that all memory accesses by a microprocessor involve lock, read, write or unlock operations on a transport control block. Appellants respectfully traverse the Examiner's assertion that all memory accesses by a microprocessor involve lock, read, write or unlock operations on a transport control block. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that all memory accesses by a microprocessor involve lock, read, write or unlock operations on a transport control block. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that all memory accesses by a microprocessor involve lock, read, write or unlock operations on a transport control block, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999).

Hence, the Examiner's reasoning does not provide reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify Appellants' Background to include the missing claim limitation of claims 1, 6 and 11. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-15. *KSR International Co. v. Teleflex Inc.*, 82 U.S.P.Q.2d 1385, 1396 (U.S. 2007); *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

## VIII. CONCLUSION

For the reasons noted above, the rejections of claims 1-15 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-15.

Respectfully submitted,
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## CLAIMS APPENDIX

1. A method for processing packets of data comprising the steps of:

receiving a packet of data;

storing a payload of said packet of data in a buffer;

reading a header of said packet of data to extract a value;

indexing in a table storing a list of transport control blocks using said value;

performing a lock operation on a transport control block in an indexed entry in said table;

performing a read operation on said transport control block;

transmitting a notification to an application to read said payload, wherein said notification comprises an address of said transport control block; and

transmitting said payload of said received packet of data to said application whereby said application does not perform a lock, read, write or unlock operation on said transport control block.

2. The method as recited in claim 1 further comprising the step of:

receiving an invocation of a function call from said application upon said application receiving said notification to read said payload.

3. The method as recited in claim 1 further comprising the steps of:

performing a write operation on said transport control block;

performing an unlock operation on said transport control block; and

transmitting an acknowledgment to a transmitting network device.

4. The method as recited in claim 3 further comprising the step of:

transmitting an indication of a change in a size of said buffer to said transmitting network device.

5. The method as recited in claim 1 further comprising the step of:

transmitting said received payload to a processor to be processed.

6. A computer program product embodied in a machine readable medium for processing packets of data comprising the programming steps of:

receiving a packet of data;

storing a payload of said packet of data in a buffer;

reading a header of said packet of data to extract a value;

indexing in a table storing a list of transport control blocks using said value;

performing a lock operation on a transport control block in an indexed entry in said table;

performing a read operation on said transport control block;

transmitting a notification to an application to read said payload, wherein said notification comprises an address of said transport control block; and

transmitting said payload of said received packet of data to said application whereby said application does not perform a lock, read, write or unlock operation on said transport control block.

7. The computer program product as recited in claim 6 further comprising the programming step of:

receiving an invocation of a function call from said application upon said application receiving said notification to read said payload.

8. The computer program product as recited in claim 6 further comprising the programming steps of:

performing a write operation on said transport control block;

performing an unlock operation on said transport control block; and

transmitting an acknowledgment to a transmitting network device.

9. The computer program product as recited in claim 8 further comprising the programming step of:

transmitting an indication of a change in a size of said buffer to said transmitting network device.

10. The computer program product as recited in claim 6 further comprising the programming step of:

transmitting said received payload to a processor to be processed.

11. A system, comprising:

a communications adapter configured to communicate with an outside network, wherein said communications adapter receives a packet of data from said outside network;

a memory unit coupled to said communications adapter, wherein said memory unit stores a table listing a plurality of transport control blocks;

a TCP protocol stack running on said communications adapter;

a TCP application running on said communications adapter;

wherein said TCP protocol stack is configured to perform the following programming steps:

storing a payload of said packet of data in a buffer in said memory unit;

reading a header of said packet of data to extract a value;

indexing in said table using said value;

performing a lock operation on a transport control block in an indexed entry in said table;

performing a read operation on said transport control block;

transmitting a notification to said TCP application to read said payload, wherein said notification comprises an address of said transport control block; and

transmitting said payload of said received packet of data to said TCP application whereby said TCP application does not perform a lock, read, write or unlock operation on said transport control block.

12. The system as recited in claim 11, wherein said TCP protocol stack is further configured to perform the following programming step

receiving an invocation of a function call from said TCP application upon said TCP application receiving said notification to read said payload.

13. The system as recited in claim 11, wherein said TCP protocol stack is further configured to perform the following programming steps:

performing a write operation on said transport control block;

performing an unlock operation on said transport control block; and

transmitting an acknowledgment to a transmitting network device.

14. The system as recited in claim 13, wherein said TCP protocol stack is further configured to perform the following programming step:

transmitting an indication of a change in a size of said buffer to said transmitting network device.

15. The system as recited in claim 11 further comprising:

a processor coupled to communications adapter;

wherein said TCP application is configured to perform the following programming step:

transmitting said received payload to said processor to be processed.

## EVIDENCE APPENDIX

No evidence was submitted pursuant to §§1.130, 1.131, or 1.132 of 37 C.F.R. or of any other evidence entered by the Examiner and relied upon by Appellants in the Appeal.

## RELATED PROCEEDINGS APPENDIX

There are no related proceedings to the current proceeding.

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